In Re Patent Application of:
D'ALBORE ET AL.
Serial No. **10/820,462**
Filing Date: **April 8, 2004**

REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. The independent claims have been amended to more clearly define the present invention over the cited prior art references. In particular, independent Claims 1, 16 and 25 have been amended to include the subject matter from their respective dependent Claims 13-14, 23-24 and 32-33. These dependent claims have been cancelled. The claim amendments and arguments supporting patentability of the claims are provided below.

I. The Amended Claims

The present invention, as recited in amended independent Claim 1, for example, is directed to a method for patching read only memory (ROM) instructions in an electronic system comprising a first non-volatile memory portion storing instruction groups defining patching functionalities, an extended memory portion storing extended instructions, and an additional memory portion.

The method comprises checking a flag stored in the additional memory portion. The flag indicates a need for executing the extended instructions in the extended memory portion. Processing of the ROM instructions in the first non-volatile memory portion and the extended instructions in the extended memory portion are alternated based upon the flag. The flag represents binary information associated to a subroutine that uses a patching mechanism defined by the ROM instructions,

with each patching mechanism having a respective flag associated therewith.

Independent method Claim 16 has been amended similar to amended independent method Claim 1. Independent device Claim 25 has been amended similar to amended independent method Claim 1.

II. The Claims Are Patentable

The Examiner rejected independent Claims 1, 16 and 25 over the Wong et al. published patent application. Wong et al. discloses a programmable memory that stores patches and vectors to determine a patch address. Reference is directed to paragraph 7 of Wong et al., which provides:

> "An embedded ROM-based processor system according to an embodiment of the present invention includes a processor, system memory, a programmable memory, a data selector and a patch controller. The system memory includes a read-only memory (ROM). The programmable memory stores patch information including patch code and one or more patch vectors. Each patch vector includes a break-out address from the ROM and a patch-in address to a corresponding location within the patch code. The patch controller is operative to compare an address provided by the processor with each break-out address to determine a breakout condition, and to control the selector to transfer the processor to a corresponding location within the patch code in response to a break-out condition." (Emphasis added).

In sharp contrast, the claimed invention recites that the flag represents binary information associated to a subroutine that uses a patching mechanism defined by the ROM instructions, with each patching mechanism having a respective flag associated therewith. An advantage of the clamed invention is that there is an interaction between the first non-volatile memory portion storing the instruction groups defining patching functionalities, the extended memory portion storing extended instructions, and the additional memory portion - in which the patching mechanism starts from the software module that requires to be patched (or to be extended), and therefore, from the application code (ROM).

The claimed invention thus avoids the use of patch vectors. In the claimed invention, instructions are predisposed for the patching according to which it is possible to call indirectly a patch (or extension) into the non-volatile memory. An advantage in avoiding the use of patch vectors is to avoid comparisons of break-out addresses with addresses provided by the processor. As noted above in Wang et al., the patch mechanism starts from a patch controller that is operative to compare an address provided by the processor with each break-out address.

It is further noted that Wong et al. needs to map a portion of the patch code. Paragraph 33 of Wong et al. provides: "In this case, the patch code 420 located in the RAM 406 is outside the allowed operation instruction space of the UPC 402. In this case, the patch code 420 is mapped into unused ROM space". (Emphasis added). In sharp contrast, the claimed invention does not need to map any portion of patch code.

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In conclusion, Wong et al. describes a low-level patch approach based on an electronic embedded architecture, and patch codes that can modify the ROM codes. In sharp contrast, the claimed invention provides an application level patch approach adapted for execution flow flags that modify specific ROM codes.

Accordingly, it is submitted that amended independent Claim 1 is patentable over the Wong et al. published patent application. Amended independent Claims 16 and 25 are similar to amended independent Claim 1. Therefore, it is submitted that these claims are also patentable over the Wong et al. published patent application.

In view of the patentability of amended independent Claims 1, 16 and 25, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

III. CONCLUSION

In view of the claim amendments and arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the Commissioner for Patents on this 7 day of May, 2007.